Appl. No. 10/644,226
Amdt. dated December 2, 2003
Preliminary Amendment

PATENT

Amendments to the Claims:

this listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1 - 26. (Canceled)

1   27.   (New) A data processing unit comprising:

2   an instruction cache to store instructions for execution, including instructions

3 belonging to an M-bit instruction set and instructions belonging to an N-bit instruction set, where

4 $M < N$;

5   an instruction fetch unit coupled to receive instructions from the instruction cache,

6 and operable to produce control signals representative of decoded N-bit instructions; and

7   one or more execution units coupled to the receive the control signals from the

8 instruction fetch unit,

9   the instruction fetch unit comprising a translation unit to translate an M-bit

10 instruction received from the instruction cache to produce one or more N-bit instructions,

11   the instruction fetch unit further comprising a decoder unit to decode only N-bit

12 instructions, thereby producing the control signals, the translation unit configured to deliver the

13 one or more N-bit instructions to the decoder unit,

14   wherein the M-bit instruction set includes data instructions that produce M-bit

15 results,

16   wherein the N-bit instruction set includes first data instructions that produce N-bit

17 results and second data instructions that produce M-bit results,

18   wherein the instruction fetch unit is configured to produce one or more of the

19 second data instructions in response to receiving an M-bit data instruction.

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1   28.   (New) The data processor unit of claim 27 wherein the second data

2   instructions further store the M-bit results into an N-bit data store and perform sign-extension of

3   the M-bit result in the N-bit data store to produce an N-bit result.

1   29.   (New) The data processor unit of claim 27 wherein the instruction fetch

2   unit includes a pre-decoder unit configured to receive N-bit instructions from the instruction

3   cache and to produce one or more pre-decode signals in response to a received N-bit instruction,

4   the pre-decoder unit providing a signal path to deliver the received N-bit instruction and the one

5   or more pre-decode signals to the decoder, wherein the translation unit is further configured to

6   produce corresponding pre-decode signals associated with the one or more N-bit instructions and

7   to deliver the corresponding pre-decode signals to the decoder, wherein the corresponding pre-

8   decode signals are pre-decode signals that would be produced if the one or more N-bit

9   instructions were processed by the pre-decoder unit.

1   30.   (New) The data processor unit of claim 27 wherein M is 16, and N is 32.

1   31.   (New) A data processor comprising:

2   first means for caching instructions for execution, the instructions comprising

3   instructions of an M-bit instruction set and instructions of an N-bit instruction set, where M < N;

4   second means for decoding M-bit instructions received from the first means to

5   produce one or more N-bit instructions corresponding to an M-bit instruction;

6   third means for decoding N-bit instructions to produce control signals, wherein

7   the N-bit instructions can be received from the first means or the second means; and

8   one or more execution units configured to receive the control signals, thereby

9   executing the N-bit instructions,

10   wherein the M-bit instruction set includes data instructions for operating on M-bit

11   data,

12   wherein the N-bit instruction set comprises first data instructions for operating on

13   N-bit data and second data instructions for operating on M-bit data,

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1   32.   (New) The data processor of claim 31 wherein the data instructions in the

2   M-bit instruction set produce M-bit results, wherein the first data instructions of the N-bit

3   instruction set produce N-bit results, and wherein the first data instructions of the N-bit

4   instruction set produce M-bit results.

1   33.   (New) The data processor of claim 32 wherein the second means is

2   further for producing one or more of the second data instructions of the N-bit instruction set in

3   response to receiving a data instruction from the M-bit instruction set.

1   34.   (New) The data processor of claim 31 wherein the second means is

2   further for producing first pre-decode signals associated with the one or more N-bit instructions,

3   wherein the third means comprises a decoder means for producing the control signals and a pre-

4   decoder means for producing second pre-decode signals, wherein the decoder means is

5   responsive to the first pre-decode signals and to the second pre-decode signals.

1   35.   (New) The data processor of claim 31 wherein M is 16 and N is 32.

1   36.   (New) A microprocessor comprising:

2   a memory for storing instructions, the instructions comprising M-bit instructions

3   and N-bit instructions, where M < N;

4   a translation circuit for receiving M-bit instructions from the memory, the

5   translation circuit configured to produce one or more N-bit instructions in response to a received

6   M-bit instruction and to produce corresponding pre-decode signals associated with the one or

7   more N-bit instructions;

8   a predecoder circuit for receiving N-bit instructions from the memory, the

9   predecoder circuit configured to produce associated pre-decode signals in response to a received

10   N-bit instruction; and

11   a decoder circuit for receiving the one or more N-bit instructions and the

12   corresponding pre-decode signals from the translation circuit and further for receiving the

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13 received N-bit instruction and the associated pre-decode signal from the predecoder circuit,

14 wherein control signals are produced in response thereto,

15   wherein the pre-decode signals corresponding to the one or more N-bit

16 instructions that are produced by the translation circuit are the same pre-decode signals that

17 would be produced if the one or more N-bit instructions were received by the predecoder circuit.

1   37.   (New) The microprocessor of claim 36 wherein the N-bit instructions

2 include first data instructions for processing N-bit data and second data instructions for

3 processing M-bit data, wherein one or more of the second data instructions are produced by the

4 translation circuit in response to receiving an M-bit instruction that is a data instruction.

1   38.   (New) The microprocessor of claim 37 wherein the second data

2 instructions produce M-bit results.

1   39.   (New) The microprocessor of claim 38 wherein the second data

2 instructions further store the M-bit results in an N-bit data store and perform a sign-extension

3 operation to produce an N-bit result.

1   40.   (New) The microprocessor of claim 36 wherein M is 16 and N is 32.